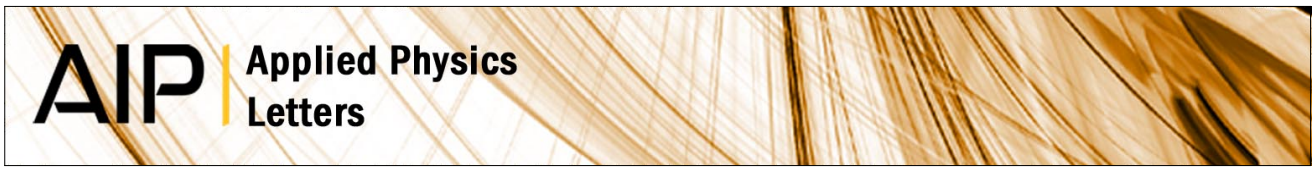

Metal-high-k-high-k-oxide-semiconductor capacitors and field effect transistors using Al/La2O3/Ta2O5/SiO2/Si structure for nonvolatile memory applications

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Metal-high-*k*-high-*k*-oxide-semiconductor capacitors and field effect transistors using $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ structure for nonvolatile memory applications

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A metal-high-*k*-high-*k*-oxide-silicon structure was fabricated for nonvolatile memory applications. $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ capacitors and field effect transistors were fabricated using Ta_2O_5 as the charge storage layer and La_2O_3 as the blocking layer. The programing time of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors was characterized. With a programing pulse voltage of 6 V, a threshold voltage shift of more than 0.5 V was achieved in 10 ns. As for the retention properties, the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors can keep a ΔV_{th} window of 0.83 V for 10 yr. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2800821]

SONOS (polysilicon-oxide-nitride-oxide-silicon) flash memory is one of the most attractive candidates for nonvolatile memories. It has the advantages of lower programing voltage, smaller cell size, and better endurance over the floating-gate devices. The faster programing speed and lower operating voltage of SONOS devices were accomplished in the past by reducing the tunnel oxide thickness.[1–4] However, the retention time and erase speed remain as the two major problems of SONOS flash memory. Several efforts have been made to improve the retention time of SONOS devices. She *et al.*[5] used HfO_2 to replace Si_3N_4 and obtained a higher conduction band offset for better retention. Minami *et al.*[6] improved retention by using blocking oxide and Bu *et al.*[7] improved retention by high-temperature deuterium annealing. Choi *et al.*[8] and Lee *et al.*[9] improved program/erase speed and retention by using high-*k* dielectrics as the blocking oxide. Tan *et al.*[10] compared the Si_3N_4, HfO_2, and HfAlO layers for the charge storage layer and found that the large conduction band offset can improve program speed and minimize the over-erase phenomenon. Wang *et al.*[11,12] improved retention time and program speed by using the $TaN/HfO_2/Ta_2O_5/HfO_2/Si$ (MHTHS) and $TaN/Al_2O_3/Ta_2O_5/HfO_2/Si$ (MATHS) structures to replace the traditional SONOS structure.

In this work, metal-high-*k*-dielectric-high-*k*-dielectric-oxide-silicon (MHHOS) capacitors and field effect transistors were fabricated using Ta_2O_5 as the charge storage layer and La_2O_3 as the blocking oxide. The potential advantages are fast programing time and low program/erase voltage. Figure 1 shows the energy band diagrams of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistor under (a) positive and (b) negative gate biases. In order to construct all band diagrams, the work functions of Ta_2O_5, La_2O_3, and HfO_2 must be 3.2, 1.75, and 2.05 eV, respectively.[13,14] The conduction band offset between the tunneling oxide and the high-*k* dielectric layer is 2.25 eV for the Ta_2O_5/SiO_2 interface.[13] The large conduction band offset is expected to improve the programing speed and the retention properties. A deep trap level in Ta_2O_5 was reported at 2.7 eV (Ref. 15) below the conduction band edge which is much deeper than the 1 eV trap level in Si_3N_4. A deeper trap level is expected to help retention. La_2O_3 is chosen to be the blocking oxide due to its high dielectric constant of about 25 and its large conduction band offset of 1.45 eV at the Ta_2O_5/La_2O_3 interface. The large conduction band offset is expected to give better blocking efficiency which will improve memory window and programing speed. High-*k* blocking layer is also expected to reduce the program/erase voltage.

p-type, (100) orientation, 4 in. diameter silicon wafers with 1–10 Ω cm resistivity were used as the starting substrates. A 3 nm tunneling oxide (SiO_2) was thermally grown by dry oxidation at 900 °C. The charge storage layer (Ta_2O_5) was deposited by rf magnetron sputtering under a pressure of 1.1×10^{-3} torr at room temperature in argon gas. The purity of Ta_2O_5 target is 99.9%. The thickness of the Ta_2O_5 layer is 20 nm. The Ta_2O_5 films were either as deposited or annealed at 400, 500, and 600 °C. The annealing was performed in nitrogen at a flow rate of 3 SCCM (SCCM denotes standard cubic centimeters per minute at STP. After annealing, the blocking layer La_2O_3 was deposited by rf magnetron sputtering under a pressure of 1.1×10^{-3} torr at room temperature in argon gas. The thickness of the La_2O_3 blocking layer is 20 nm. For transistor processing, a 500 nm oxide was grown by wet oxidation and used as the field oxide. The source and drain windows were defined by wet etching and doped by arsenic implantation (5×10^{15} cm^{-2},40 keV). The implant was annealed at 950 °C in N_2 for 30 min. The contact region in Ta_2O_5 was etched by

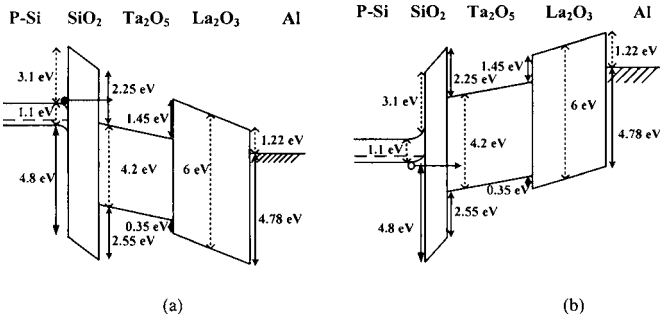

FIG. 1. The energy band diagrams of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistor under (a) positive and (b) negative gate biases.

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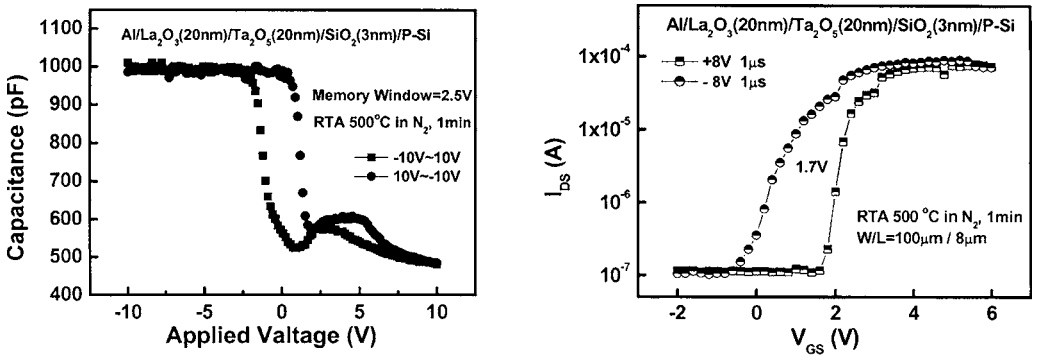


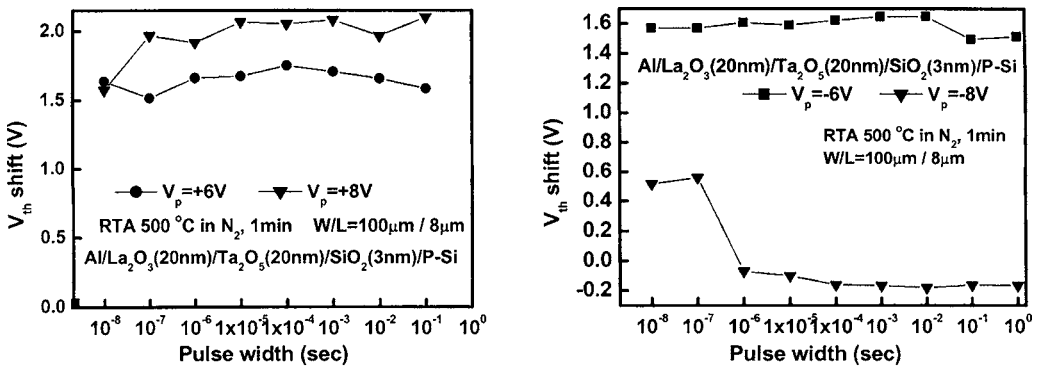
(a) (b)

FIG. 2. *C-V* memory window. (b) I_{DS}-V_{GS} memory window.

reactive ion etch and in SiO_2 and La_2O_3 by buffered oxide etch. The 300-nm-thick top aluminum electrodes were evaporated by dc sputtering. Postmetallization annealing was performed at 400 °C in N_2 for 30 s. The crystalline phase of the high-*k* dielectric films was identified by x-ray diffraction (Shimatzu XD-5) using Cu $K\alpha$ radiation. From the x-ray diffraction results, the Ta_2O_5 film is amorphous after annealing. Separate MHHOS capacitors were also fabricated. The *I-V* characteristics were measured using Keithley 236 electrometer and the *C-V* characteristics using high frequency *C-V* meter MegaBytek Mi-494.

Figure 2(a) shows that the capacitance-voltage (*C-V*) hysteresis curves for the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ capacitors. At a sweep voltage range of ±10 V, the *C-V* memory window is 2.52 V. The *C-V* memory window is counterclockwise because the trapped charges are electrons. Figure 2(b) shows the I_{DS}-V_{GS} memory window measurement for $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors with channel width/length of 100 μm/8 μm. The rising time and falling time of pulse wave are both 39 ns. The I_{DS}-V_{GS} memory window after a 8 V, 1 μs program pulse is 1.7 V. The difference between the *C-V* memory window of 2.52 V and the I_{DS}-V_{GS} memory window of 1.7 V is most likely due to process variation, since they were processed differently.

Figure 3(a) shows the program characteristics of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors. Pulse voltages of 6 and 8 V are applied to the gate. The pulse widths are from 10^{-8} to 1 s. After applying the gate pulse, the threshold voltage of the transistor was monitored. V_{th} is defined as the gate voltage at 1 μA drain current with V_{DS}=0.1 V. The transistor is defined as "programed" when the V_{th} shift is larger than 0.5 V. For $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors, the V_{th} shift of more than 0.5 V will occur at an applied voltage of 6 V and with a pulse width of 10 ns. For MHTHS (Ref. 11) and MATHS,[12] the V_{th} shift of more than 0.5 V will occur at an applied voltage of 10 V and with pulse widths of 1 ms and 100 ns, respectively. Therefore, low program voltage and fast programing speed were achieved with $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors. The $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors thus have faster programing speed and lower program voltage than MHTHS and MATHS. This is most likely due to the larger conduction band offset of 2.25 eV at the Ta_2O_5/SiO_2 interface compared with 1.2 eV at the Ta_2O_5/HfO_2 interface. At the same gate bias where Fowler-Nordheim tunneling is dominating, the electron tunneling distance from Si substrate to the conduction band of the storage dielectric is, therefore, shorter for structures with Ta_2O_5/SiO_2. The program voltage of $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistor can be as low as 6 V, which is lower than that of 10 V for MHTHS (Ref. 11) and MATHS.[12] The programing time of 10 ns is also faster than those of 1 ms and 100 ns of MHTHS and MATHS, respectively. Figure 3(b) shows the erase characteristics of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors. The transistor is defined as "erased" when the V_{th} reduced to 0 V. Based on this definition, an applied gate voltage of −6 V is not enough for erased while the V_{th} reduced to 0 V at an applied voltage of −8 V with a pulse width of 1 μs.



(a) (b)

FIG. 3. (a) The programing characteristics of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors. (b) The erase characteristics of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors.

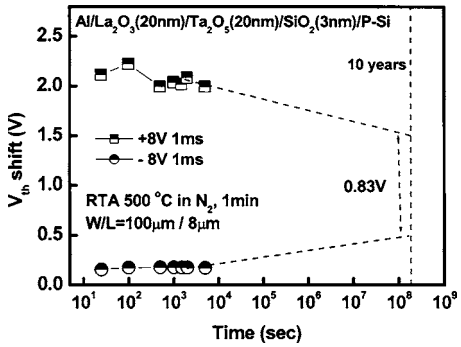


FIG. 4. The retention properties of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors.

Figure 4 shows the retention characteristic of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors. The I_{DS} vs V_{GS} characteristic was measured with a sweep voltage from −3 to 3 V to determine the original threshold voltage. Pulse voltages of ±8 V at 1 ms duration were then applied for program and erase operations. The threshold voltage shift is measured at different time periods. The linear extrapolation was performed by using the last two data points of V_{th} measurements. The same method is also used for the erase state. The $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors are projected to have a ΔV_{th} window of 0.83 V after 10 yr.

In summary, $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ capacitors and transistors were fabricated. The electrical properties, including *C-V* memory window, I_{DS}-V_{GS} memory window, program/erase characteristics, and retention time were measured. At a sweep voltage range of ±10 V, the *C-V* memory window is 2.52 V. The I_{DS}-V_{GS} memory window after ±8 V, 1 μs programing pulses is 1.7 V. The V_{th} shift of the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors at an applied gate voltage of 6 V and with a pulse width of 10 ns is 1.6 V. As for retention properties, the $Al/La_2O_3/Ta_2O_5/SiO_2/Si$ transistors are projected to have a ΔV_{th} window of 0.83 V after 10 yr.

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